Expression of Intent for
PIX00: A pixel system at the
inner radius of CDFII for Run IIb

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1 Pixel Option for Layer00

1.1 Overview
An option exists to replace the Layer00 silicon microstrip detector with a pixel detector. This option makes use of advanced R&D by the LHC experiments and the BTeV experiment. The proposal is to form a single layer of pixels using ATLAS-style sensors. The sensors will be bump-bonded to a FPIX readout chip. ATLAS sensors are in production and the FPIX readout chip exists in an advanced third generation prototype that has been developed at Fermilab. In fact, a prototype system (ATLAS-style sensors + FPIX chips) was successfully tested during the last test beam run at Fermilab using CDF SVX readout electronics (STAR+VRB). Position resolution better than 10 \( \mu m \) was demonstrated.

The proposed geometry includes 12 staves each 75 cm long and about 1 cm wide. The staves are arranged 12-fold in \( \phi \) to form a single barrel layer. A stave consists of 12 sensors with each sensor read out by 8 FPIX chips. The detector comprises 144 sensors and 1152 readout chips. An individual pixel is small: 50 \( \mu m \times 400 \mu m \). In total, the detector contains 3.3 M channels.

This description of a pixel option to replace Layer00 represents our current understanding of the proposed system. Work continues on refining the numbers that appear such as the material budget and cost estimate. A future document with all figures fully referenced will follow.

1.2 Physics Motivation and Tracking Performance
For a Standard Model Higgs discovery and for discovery of several types of SUSY signatures, \( b \)-tagging efficiency is very important. Pixels provide excellent position resolution (6-10 \( \mu m \) depending upon the incident track angle) in \( r-\phi \) similar to strips. In addition, pixels provide several other attractive features. First, pixels provide fine segmentation in \( z \) that can be used for pattern recognition. Approximately 30\% of the charged tracks from \( b \)'s in top events have shared hits on Layer00 strips. For pixels, approximately 90\% of these overlaps would be resolvable due to the segmentation in \( z \). Second, pixels provide a precision \( z \)
measurement that could have a resolution of 200 $\mu$m/$\sqrt{2}$ assuming the pixels are staggered and that charge is shared between two pixels. Third, pixels are more tolerant to radiation ($\sim 30$ Mrad $\equiv 30$ fb$^{-1}$) and would require only the single installation even if the accelerator delivers luminosity exceeding current expectations of 15 fb$^{-1}$. With large uncertainties, Layer00 strips are expected to last to 10 fb$^{-1}$. In short, at the Layer00 radius, the radiation environment is very similar to an LHC environment. Pixels are the best technology choice at this time for providing high precision tracking in such a high radiation environment.

1.3 Sensors

ATLAS has chosen pixel sensor technology that has achieved high performance out to about 30 Mrad of radiation dose. The 50 $\mu$m $\times$ 400 $\mu$m pixels are composed of n$^+$-type implants on n-type bulk with a p-spray isolation. A series of guard rings is also employed. The end result is a sensor that after type inversion and 30 Mrad of dose can use a 600 V bias to collect approximately 2/3 of the charge that is collected by an un-irradiated sensor.

The ATLAS experiment has selected two vendors (Cis and Tesla) to produce their needs of about 3000 wafers of sensors. The CDF pixel system would require about 50 wafers assuming a yield of 50% or 100-150 total wafers if sensors are shared between D and/or BTeV. It is reasonable that sensors with the ATLAS-style specifications could be ordered with a CDF-style geometry in the Fall of 2001.

1.4 FPIX readout chip and DAQ

The Fermilab rad hard vertex group has worked with the BTeV group and Ray Yarema’s ASIC design group to develop a pixel readout chip that is suitable for use by experiments at the Tevatron. It is anticipated that a CDF pixel system could use a readout chip which is either identical to or only slightly different from the one being developed for BTeV. The current prototype version of the chip has a final-design core (amplifiers and digitization for each pixel cell) already qualified in a deep submicron process ($0.25 \mu$m). Radiation testing at a Co-60 facility to 30 Mrads shows little or no degradation. A next prototype will be submitted at the end of September 2000 and will contain a periphery that tests several options for communication between the pixel chip and the DAQ. The FPIX readout chip development has gone very well. In some sense, by choosing early to use a deep submicron process, the FPIX chip is more advanced than the LHC pixel readout chips. It is reasonable that production chips could also be ordered in the Fall of 2001.

The FPIX chip has a different readout scheme compared with the SVX3 chip. In particular, pixel hits are stored within each pixel cell with a beam crossing number, BCO. Every hit gets read out with row and column information, the BCO, and 3 bits of digitized analog information. The concept is that the pixel detector will send all the data to a deep memory module that will sort pixel hits by BCO and will match L1 accepts with the correct BCO. The module will then provide pixel data to a VRB module for readout. A concept also exists for this module to combine pixel hits back into effective strips to provide data to the SVT with no hardware changes to the SVT. This deep memory module will also provide the control signals to the FPIX chip (it is equivalent to the FIB module). The deep memory/pixel-FIB would be a new module that would need to be developed. The control of the FPIX is simpler than SVX3 so the scale of producing this module is estimated to be equal to the scale for FIB development.
Various other aspects of the pixel DAQ including a pixel port card are under development within the same Fermilab ESE group that designed the SVX DAQ. The pixel port card would be expected to contain commercial optical drivers and would sit outside the tracking volume in a not-so-intense radiation environment. A HDI cable would connect FPIX chips on the sensors with the port card. Prototype components of this DAQ are currently under test by the ESE group.

1.5 Mechanical Design, Cooling, and Material Budget

A pixel detector module for CDF would consist of a $8 \times 64$ mm$^2$ silicon sensor with 8 bump-bonded readout chips. A Kapton hybrid circuit would be attached to the top of the sensor to bus signals to and from the readouts via wire bonds. The wire bonds would be encapsulated to prevent damage by interconnecting cables. The pixel size would be $50 \mu m \times 400 \mu m$.

Similar modules have been successfully constructed and tested in the Fermilab FPIX program using ATLAS sensors and FPIX readout chips. Fig. 2 shows 5 FPIX chips bump bonded to an ATLAS sensor, which is designed to be read out by 16 chips in two rows. As stated above, the CDF pixel modules would have one row of 8 chips. A test board is shown in Fig. 2. The readout chips are underneath the sensor with their bond pads extending beyond its edge. The Kapton flex circuit is also attached to the board in this prototype. At a later stage, the chips will be connected to a narrower flex circuit mounted on top of the sensor, as in the final design.

The basic mechanical support and cooling structure is based on the relatively mature ATLAS design. It consists of a barrel made of 12 “staves” holding 12 detector modules each. The active length of each stave is approximately 75 cm, which is shorter than the ATLAS staves (1 m). A cross section of a stave is shown schematically in Fig. 3. The stave includes a long carbon-carbon heat conducting bar to which the detector modules are attached. A thin-walled aluminum cooling pipe runs the length of the bar and is held in place by a carbon fiber-epoxy “omega” channel which provides rigidity. Thermally conductive grease is used to provide thermal contact between the aluminum tube and the carbon-carbon bar. The bar, omega channel and silicon detector module have similar CTEs. The CTE of the aluminum tube is sufficiently different that it must not be rigidly attached to the bar. There will be intermediate supports between the staves and the beam pipe at two points along the length of the staves to prevent excessive bowing. ATLAS has found the need to provide 3 or 4 external supports along the length to compensate for gravitational sag.

Two possible configurations of the staves to form a barrel layer (tilted or staggered) are shown schematically in Fig. 4 and Fig. 5, respectively. The $10^\circ$ tilt partially compensates for the Lorentz angle of the charge carriers in the sensors. The tilted design also interposes...
Figure 2: Detector test module with 5 chips wire-bonded to 5-layer flexible circuit.

Figure 3: CDF pixel detector stave concept (cross section). The active area of the sensor is shown in color.
less material on average between the beam pipe and the first sensor layer. The barrel staves must be positioned to avoid contact with the “flag” on the underside of the beam pipe.

The Kapton cables to connect the detector modules to the outside world are attached to the surface of the hybrid circuit and routed tangentially outward to the region outside the barrel layer where they make a right angle and proceed along the barrel next to the omega channel of the neighboring stave.

The power dissipation of the FPIX chips is quite high and an adequate cooling system is required to keep most of the pixel system at low temperatures. The core of the pixel chip generates 55 μW with about an additional 20% in the periphery expected. In short, the entire pixel detector is expected to generate 250 W. The ATLAS stave design assumes a somewhat higher power dissipation by area and uses twice as many chips per unit stave length. They found that 2 mm radius cooling tubes were sufficient for their design, which also includes other complexities in terms of the coolant and distribution. We are hopeful that a simpler design using cooling tubes not much larger than 1.5 mm in radius will be more than adequate. We are in the process of simulating our heat generation and cooling scheme to confirm these expectations.

The amount of material in the pixel system is estimated to be less than 2.5% X₀. An initial study shows that very little degradation in impact parameter occurs with 2.5% X₀ compared with 1.5% X₀ of the current Layer00 design. Both ATLAS and BTeV estimate modules (no support and cooling) to be approximately 0.7% X₀ with the amount of silicon dominating (two layers of silicon are about 0.6% X₀). If one accounts for the overlap of material for radial tracks, one sees that the proposed geometry is mostly four layers of silicon or two layers of silicon with a cooling tube. Equating the cooling tube with two layers of silicon, we see the material is approximately equivalent to four layers of silicon. The addition of support, the HDI, and power cables should still result in a detector that is less than 2 or 2.5% X₀. Further details of the material budget are under study.
1.6 Resource and Cost Estimates

The resources and costs needed for completing this project are greatly reduced due to the substantial overlap with this project and BTeV’s proposed 10% scale test. For this discussion, we assume that both this proposal and a 10% BTeV test are approved (D is also considering a pixel option). For the sensors, we currently use a $2.5K per sensor estimate for an order of 100 wafers (BTeV cost estimate) to be compared with $5.5K per wafer estimate for a smaller prototype run. An additional $50K of NRE charges for the sensors is assumed. For the readout chip, both the 10% scale and the needs for CDF would each be about 10 wafers. The first 10 wafers can be purchased for $160K and the additional wafers can be purchased for $30K. For the bump bonding, we assume that bump bonding costs are equal to the sensor costs. Mechanical support and cooling costs are typically $100K for fixtures and materials. Engineering support would also be required. The HDI costs are assumed to be $50K, the pixel port card also $50K, and a pixel-FIB and other DAQ components are estimated to be $100K. The totals for CDF are $700K which agrees with an initial goal to keep the costs, including those not tabulated, for this detector below $1M.

As far as personnel resources, sufficient resources exist with the Fermilab ASIC design and rad hard vertex groups to see that production sensors and readout chips could be ordered in the Fall of 2001. For the bump bonding, we are examining UC Davis’ capabilities that have been used for prototype bonding for a large number of pixel tests including a successful test beam at SLAC this past summer. A great advantage is to have an interested party willing to put up with the schedule demands of our experiment. However, support from Fermilab would be required for fixturing and a one FTE-yr technician to perform the production work. For mechanical and cooling, we require the use of engineers and designers currently at SiDet. We assume 3 FTE-yr engineering and 2 FTE-yr technicians are required.

This project makes use of the expertise of the Fermilab rad hard vertex group and various CDF institutions actively involved in either pixel or diamond work for the LHC.
experiments. Finally, DAQ and other silicon hardware (HDIs and port cards) have also been made by CDF institutions in the past. The proposed schedule is that production sensors and chips arrive by the end of 2001. Year 2001 will also be used to complete the mechanical and DAQ design. In 2002, testing sensors/chips followed by bump-bonding will result in the completion of modules by the end of 2002. Also in year 2002, fixturing and other materials will be ordered for the mechanical construction of staves and the detector. Prototype DAQ modules will also be ordered and debugged. Year 2003 will be devoted to constructing staves and assembly of the final detector including DAQ.

1.7 Conclusions and Feasibility

The key points of proposing a replacement for Layer00 microstrips with a pixel detector are the following. First, pixels provide precision space points that extend our current capabilities by providing advantages in pattern recognition. Second, pixels are radiation hard at a level required for continuous high luminosity running (no second shutdown for another replacement). Third, a pixel detector at CDF makes use of expertise both at Fermilab within the rad hard vertex group, the ESE group, and SiDet; and makes use of expertise among CDF collaborators engaged in silicon and diamond pixel detector development for other projects. Fourth, the marginal cost of this project to the laboratory is reduced due to the overlap with plans for continued pixel development at the Tevatron and the potential for outside groups to raise money for advanced detector development. A pixel detector is the best technology choice at small radius in the collider detectors and is achievable with small marginal costs to the laboratory.