L2 Components

? **Alpha:**
- 5 operational, 1 nearly so, 3 soon
- Still shooting for 11
- Working on layout for additional 12

? **Beta:**
- Orsay contributing 2 full time engineers.
- Working to integrate
- Prototype this summer

? **MBT:** Hardware/firmware done

? **FIC:** Modifications understood.

? **CIC/SFO:** Ready for production.

Sufficient hardware in hand now a matter of integration.
Tests Results

- Using 64 channel mask (16 on/48 off to test noise/cross-talk)
- Can fit peaks to all 16 channels (See Fig.)
- With a 2PE threshold 16 fire @ 98% eff, 48 @ 0.1% eff.
- Noise about 1/3 PE. Consistent with Stereo Boards.(See Fig.)
- Up Next: 512 channels, LHB/RHB, cryo

Production

- Vendor has had layout since Feb 23. Still on track for late March completion
- Have started planning for AFE Testing/Installation
  - 3 test stands (visual/functionality/noise)
  - Requires over five people. Will call on collaboration
  - Next week will need a physicist to test software/documentation now in preparation.

Analog in good shape, need to be vigilant about full board noise tests and test stand schedule.

http://sbhepl.physics.sunysb.edu/~grannis/afe.html

Blazey NIU/FNAL
ADM March 9, 2001
L3 Hardware

? VRC composed of SIB1/VBDi needed for ~100 Hz Operation along with Ethernet upgrade

? SIB1

- Feb 16: Arrived at Brown
- Feb 23: Stuffed
- Today:
  - i960, FPGA, INOVA links all functioning.
  - Sean and Jan Hoftun will start testing driver. SIB May take up residence at Brown.

? VRCi'

- March 8: Work resumed
- March 12: Send to vendor with 3 day turnaround
- March 21: At Brown.

? Started ordering server parts.

Rapid Progress last month. Have missed March 1 deadline of VRC at Brown, but still working hard for March 28 deadline of VRC at D0

http://niuhep.physics.niu.edu/~blazey/L3ReviewCommittee.htm